UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/247,974	02/11/99	YING T	TS98-518

IM62/0516

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EXAMINER	
TRAN, B	
ART UNIT	**PAPER NUMBER**
1765	9

DATE MAILED: 05/16/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/247,974	Ying et al.
Examiner	**Group Art Unit**
Binh Tran	1765

☒ Responsive to communication(s) filed on *3/7/00*.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-26* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-26* is/are rejected.

☒ Claim(s) *3* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Objections

1. Claim 3 is objected to because of the following informalities: In line 2-3 of claim 3, "a upper layer of silicon nitride" appears to have incorrect grammar. The examiner suggests replacing "a" with --an--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Claims 1, 3, 16, 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 1 of claims 1, 16 "filling gaps in a plane **of and between** a pattern" (Emphasis added) is vague and indefinite. It is unclear what plane of the pattern applicant wish to refer.

In line 8-9 of claims 1, 16, "said interconnect lines are separated by holes having bottoms between said interconnect lines" is vague. It is unclear how the interconnect lines can be separated by holes because the interconnect line is a continuous mark to define a shape or contour whether a hole is a non-continuous cavity or opening.

In line 9-11 of claim 1, "leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines" is vague and indefinite. The examiner interprets the word "hole" mean a cavity or opening in the solid. If "the substrate is exposed **over the bottoms of said hole**" then this cavity is filled and it is not a hole anymore.

In line 3-4 of claims 3, 18 "wiring structure to be applied during the SAC process" is vague and indefinite. The word "to be" indicates something in the future. Thus, it is unclear whether the wiring structure will be applied or not during the SAC process.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 8-12, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parat et al. (US 5,731,242) in view of Lee (US 5,663,092).

Parat discloses a method of forming interconnect lines, said interconnect lines having a top surface further having sidewalls, comprising the step of

providing a semiconductor substrate said substrate having a surface (Ref 210 Fig 6);

creating a network of interconnect lines on said surface of the substrate where by the interconnect lines are separated (Ref 235 Fig 6) thereby leaving the surface of said substrate partially exposed (See Fig 6);

depositing a first layer of dielectric (270) having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor (col 6 line 1-5);

depositing a second layer of dielectric (280) having a surface over first layer of dielectric;

etching said second layer of dielectric thereby creating exposed portions of said first dielectric material (col. 6 line 25-45, Fig 9 Ref 237 and 238);

depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric (col. 6 line 46-61).

Parat is silent about the step of etching back of the first layer of dielectric.

In an interconnection method, Lee discloses the step of etching back the dielectric layer form on top of the wiring structure.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat in view of Lee by etching back the dielectric layer because etching back will remove extra portions of the dielectric layer that form during the deposition process.

Regarding to claims 2-4 Parat discloses the interconnect lines contain a lower layer of conducting material such as polysilicon (230) and an upper layer of silicon nitride (238) and said interconnect line is applied during the self-aligned contact process.

Regarding to claim 5, Parat and Lee are silent whether the dielectric layer contains high density plasma oxide. However, the use of high density plasma oxide is well known in the semiconductor art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat and Lee by utilizing high density plasma oxide for the dielectric layer because Parat and Lee are not particular about the kind of dielectric oxide

material used in their process and therefore any dielectric oxide would have been anticipated to produce an expected result.

Regarding to claim 9, Parat recites the second layer of dielectric is silicon nitride with the preferred thickness approximately 1000 Å (other thickness also possible). See col. 5 line 40-45. Parat is silent about using PECVD to deposit a layer of silicon nitride at the temperature of 440 °C. However the use of PECVD to deposit silicon nitride is well known in the art. (See prior art made of record Liaw (US 5,807,779)).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat and Jeng by utilizing PECVD at 440 °C to deposit silicon nitride because PECVD is easy and effective procedure for depositing silicon nitride.

Regarding to claims 10 Parat discloses there is other material such as aluminum oxide that can be used instead of silicon nitride (col. 8 line 3-15). The deposition of second dielectric layer covers the surface of first dielectric layer on the bottom separating said interconnect lines, further covering the surface of the first dielectric overlying the top surface of the interconnect lines (Fig 8-9).

Regarding to claims 8, 10-11, Parat is silent whether the second dielectric layer covers the partially exposed of the interconnect lines. Lee discloses the second dielectric layer (silicon nitride) covers the partially exposed of the interconnect lines.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat in view of Lee by having the second dielectric layer cover

the partially exposed of the interconnect lines because the second dielectric layer will protect the interconnect lines during the etching steps.

Regarding to claim 12, Parat discloses etching the second dielectric layer in its totality except where said second dielectric layer forms spacers on the sidewall of said interconnect lines (col 6 line 25-45).

Regarding to claim 14, Parat is silent whether depositing a layer of oxide is depositing a layer of PE-oxide or PE-TEOS. Lee discloses the use of silicon oxide or TEOS as the dielectric material that is deposited over the spacers (col. 5). Both Parat and Lee are silent whether the deposition process is plasma enhance oxide or plasma enhance TEOS. However plasma enhance TEOS is well known is the art (See Chen et al. (US 5,858,869) in prior art made of record).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat and Lee by depositing a layer of PE-oxide or PE-TEOS because Parat and Lee are not particular whether their oxide layer is deposited by plasma enhance or not, and therefore depositions by plasma enhance would have been anticipated to produce an expected result.

Regarding to claim 15, Parat discloses the step of planarizing the deposited layer of oxide. Parat is silent whether the planarization is proceeded down to the plane of the top surface of the conducting line pattern.

In an interconnect method, Lee discloses planarization is proceeded down to the plane of the top surface of the conducting line pattern thereby completing the process of creating a high-

aspect ratio pattern of conducting lines said conducting lines being separated with an intra-layer dielectric (col. 5 line 38-41).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat in view of Lee by planarizing down to the plane of the top surface of the conducting line pattern because Parat planarization will remove extra portion and smooth the surface of a dielectric layer.

5. Claims 6-7, 16-24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parat in view of Lee, and further in view of Jeng et al. (US 5,683,922).

Both Parat and Lee are silent about the use of buffered oxide etch (BOE) for etching back the first dielectric layer.

In a self-aligned contact, Jeng discloses the wet etching using 20:1 BOE etchant for dielectric layer (abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Parat and Lee in view of Jeng by utilizing buffered oxide etch for etching back the dielectric layer because BOE etchant increases the selectivity of silicon oxide/silicon nitride layer.

Claim 7, 21 further differ from the references by the specific value of etchant ratio in the BOE etchant solution. It would have been prima facie obvious to employ any of a variety of etchant ratio in the BOE solution including those claimed by applicant, this is well-known variable in the wet etching art which is known to effect both the rate and quality of the wet

etching process. Further the selection of particular values for this variable would simply involve routine experimentation.

The limitation of claims 17-20, 22-23 has been discussed in previous paragraphs (similar to the limitation of claims 2-5, 9-10). The limitation of claims 24, 26 has been discussed.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parat and Lee as applied to claim 1 above and further in view of Kasai (US 5,821,594).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parat, Lee and Jeng as applied to claim 16 above and further in view of Kasai (US 5,821,594).

Claims 13, 25 differ from Parat, Lee and Jeng by further specifying CHF_3 as the etchant gas for silicon nitride at the flow rate of 15 sccm, pressure of 15 mtorr, rf power density of about 700 watts with no magnetic field and ambient wafer temperature of 15 °C.

Kasai discloses the use of CHF_3 as the etchant gas for silicon nitride layer. Claim 13, 25 further differ from Kasai by the specific value of etchant gas flow rate, gas pressure, rf power density. It would have been prima facie obvious to employ any of a variety of etchant gas flow rate, gas pressures, rf power densities including those claimed by applicant. These are all well known variable in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would simply involve routine experimentation.

Response to Arguments

8. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chen et al. (US 5,858,869) disclose the deposition of dielectric silicon oxide using plasma enhance TEOS; Liaw (US 5,807,779) disclose deposition of silicon nitride using PECVD process.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (703) 308-1867.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

Binh X. Tran

May 9, 2000